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CMOS Design For Restoring Digital Signal In Pass Transistor Logic

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Abstract- In designing digital circuit, threshold voltage drops in NMOS pass transistor actually leads to a great signal degradation, especially for the transmission of strong logic high signals. This loss of voltage commonly represented as can negatively impact circuit performance and signal integrity. To mitigate this limitation, a new methodology is introduced that makes use of a PMOS pass transistor with a feedback loop consisting of a CMOS inverter. The PMOS transistor acts as a level restorer and pushes the output voltage to the full Vdd level, compensating for the voltage loss that NMOS based circuits would be incurred. A comparative analysis is being done by using LTspice to compare the performance of the conventional NMOS pass transistor with the proposed technique. Signal degradation and propagation delay are the main focus in this analysis. The performance of this technique was validated through LTspice simulations, which showed significant improvement in signal restoration and transmission efficiency. While the proposed technique increases the circuit complexity and the number of transistors and hence increasing the area footprint, it effectively enhances the signal integrity and reduces the propagation delay. These advantages make it a reliable solution for high-performance digital applications where maintaining signal quality is essential.

Keywords:- *NMOS pass transistor, Threshold voltage drop, Level restorer, CMOS inverter, Signal integrity, Propagation delay, LTspice simulation, Digital circuit design, PMOS pass transistor, Feedback loop*

I. Introduction

In a logic circuit diagram, it may be required to add level restoration circuitry in to a circuit in order to restore a signal to a valid logic level. For instance, a very long routing path in an integrated circuit can attenuate a high logic signal due to the impedance of the routing trace, heavily loaded lines also tend to attenuate a valid logic high signal. This issue also arises in pass gate logic designs that consist of several transistors coupled in series. Due to the threshold voltage drop across transistors. Pass transistor logic (PTL) also referred to as transmission gate logic is founded on the utilization of mosfets as switches instead of as inverters [1]. The outcome is conceptual simplification but the CMOS inverter's rigorous logic-high/logic-low output characteristics is lost. One NMOS transistor can be used as a PTL switch; the switch is regarded as closed when voltage applied at the gate is logic high, and as open when voltage applied at the gate is logic low. The diagram below depicts an AND gate with only one transistor shown in figure 1. The output (Y) is logic high when the input (A) is logic high and the switch-control signal (B) is logic high, and it is not logic high for any other combination. The issue with this circuit is that the circuit doesn't assert a logic low when the B input is logic low. It's just disconnected, i.e., floating. In order to create a logic low, we require a pull-down resistor connected as shown in figure 2 [2,3].

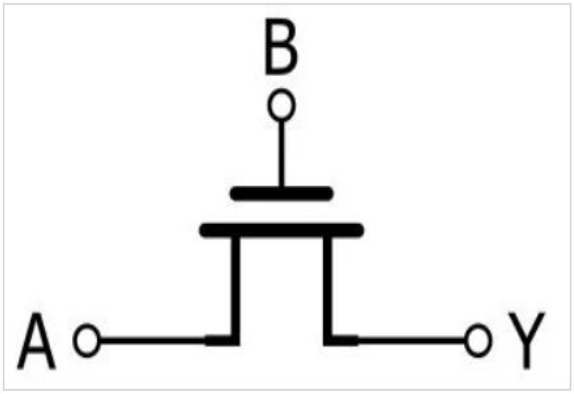

Figure1: AND gate using one transistor.

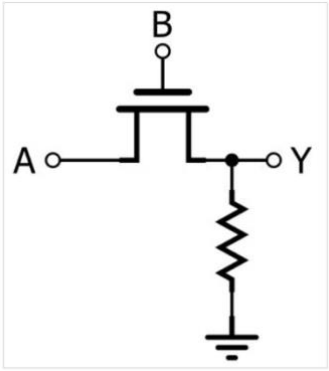

Figure2: AND gate using one transistor and one resistor

Now we have a working AND gate, and we've only used one transistor and one resistor. The issue with this circuit is that it does not consistently give a low-resistance path to ground. It dissipates static power whenever the output is logic high current flows from the input through NMOS, through the pull-down resistor to ground as shown in figure 3.

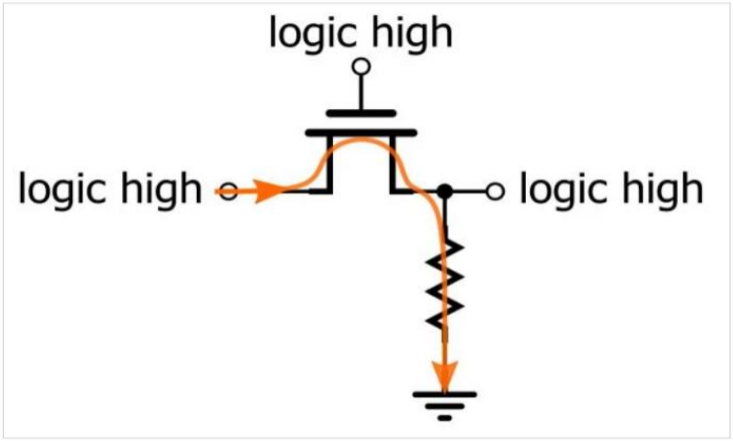

Figure 3:Working of an AND gate using one transistor and one resistor

As shown in the above section, PTL is constructed around MOSFET switches that pass or short out a signal. Implementing an NMOS transistor as the switch is indeed a good reduction of transistor count, but a single NMOS is not impressive from a performance perspective [4]. Far better is the CMOS transmission gate.

II. LITERATURE SURVEY

NMOS as a switch

An NMOS transistor is not a suitable device for logic-level switching circuits. The catch in this case is that the presence of a path for current is contingent on the availability of a gate voltage greater than source voltage. This can be easily circumvented if the circuit can tap into a control voltage that is greater than the voltage levels that will be switched through the switch. But in the case of a typical digital circuit, we can never hope to have more than two voltages: the logic-high voltage and the logic-low voltage. Circuit diagram of NMOS switch is shown in figure 4. Therefore, if you put a 3.3 V signal on the gate, the FET just can't pass a 3.3 V signal from input to output. An NMOS switch passes a "weak" one and a "strong" zero [5]. When the gate (to enable the switch) is driven logic-high and the input terminal is driven logic-low, the gate voltage is substantially greater than the two other terminals voltage. This creates a low-resistance channel from input to

output. It is quite different, however, when we drive the input terminal with a logic-high voltage. We now do not have a huge voltage difference between the gate and the remaining two terminals, and electrical performance degrades with increasing channel resistance[6]. We can use following LTspice circuit to try out the response of a NMOS switch. A control signal of 3.3 V is driven into the gate, and the input signal swings between ground and 3.3 V. The minimal load capacitance is the input capacitance of the downstream circuitry. You can observe that the slope of the output signal significantly reduces when the difference between the gate voltage and the output voltage falls below a certain threshold. The output voltage starts increasing very slowly, and it does not come close to the logic-high voltage prior to the start of the next cycle. There is also a considerable delay in the negative transition, although the output voltage does reach ground eventually. This plot should give you a good sense of what we mean by "strong" zero and "weak" one [7,8].

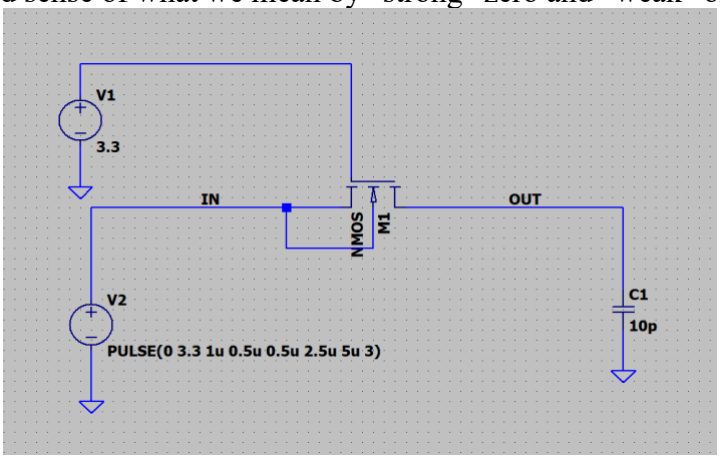

Figure 4: Circuit diagram of NMOS as a switch

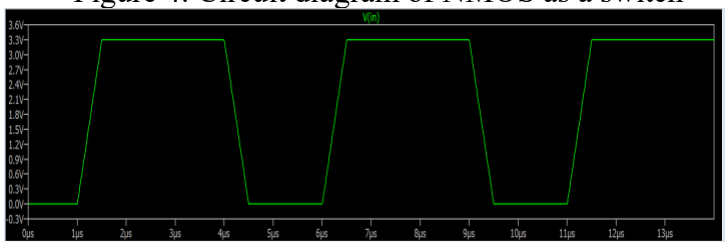

Figure 5: Input characteristics of NMOS as a switch

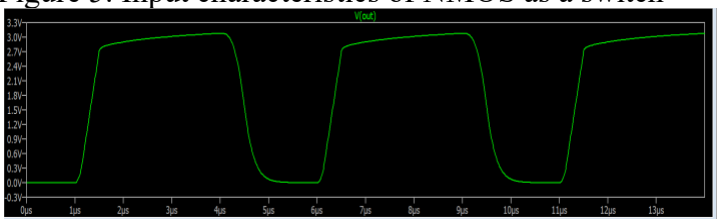

Figure 6: Output characteristics of NMOS as a switch

III. Proposed Technique

The proposed technique addresses the problem of threshold voltage drop through LTspice modelling. It rejuvenates signal loss by employing a CMOS inverter and feedback mechanism coupled to a PMOS pass transistor as shown in figure 7.

In this method, the gate of the NMOS pass transistor is fed with voltage V1(Vdd), whereas its source terminal is coupled to voltage V2. The drain of the NMOS pass transistor is connected to the source of PMOS. Concurrently, the gate of the PMOS pass transistor is linked with the feedback output of the CMOS inverter circuit. The source of the PMOS pass transistor is wired to voltage V1, while its drain goes to the input of the CMOS inverter. Because the gate of the PMOS transistor is controlled by the inverter output, circuit provides controlled feedback path.

NMOS transistors can only pass weak logic high signals because of the threshold voltage drop, with the highest output voltage being |Vdd - Vtn|, where Vtn is the threshold voltage. In order to compensate for this drop, a level restoration circuit is added. The source of the PMOS pass transistor is connected to the inverter input,

and its drain is connected to Vdd, making the PMOS transistor the level restorer. The circuit diagram of proposed technique is shown in figure 7 [9,10].

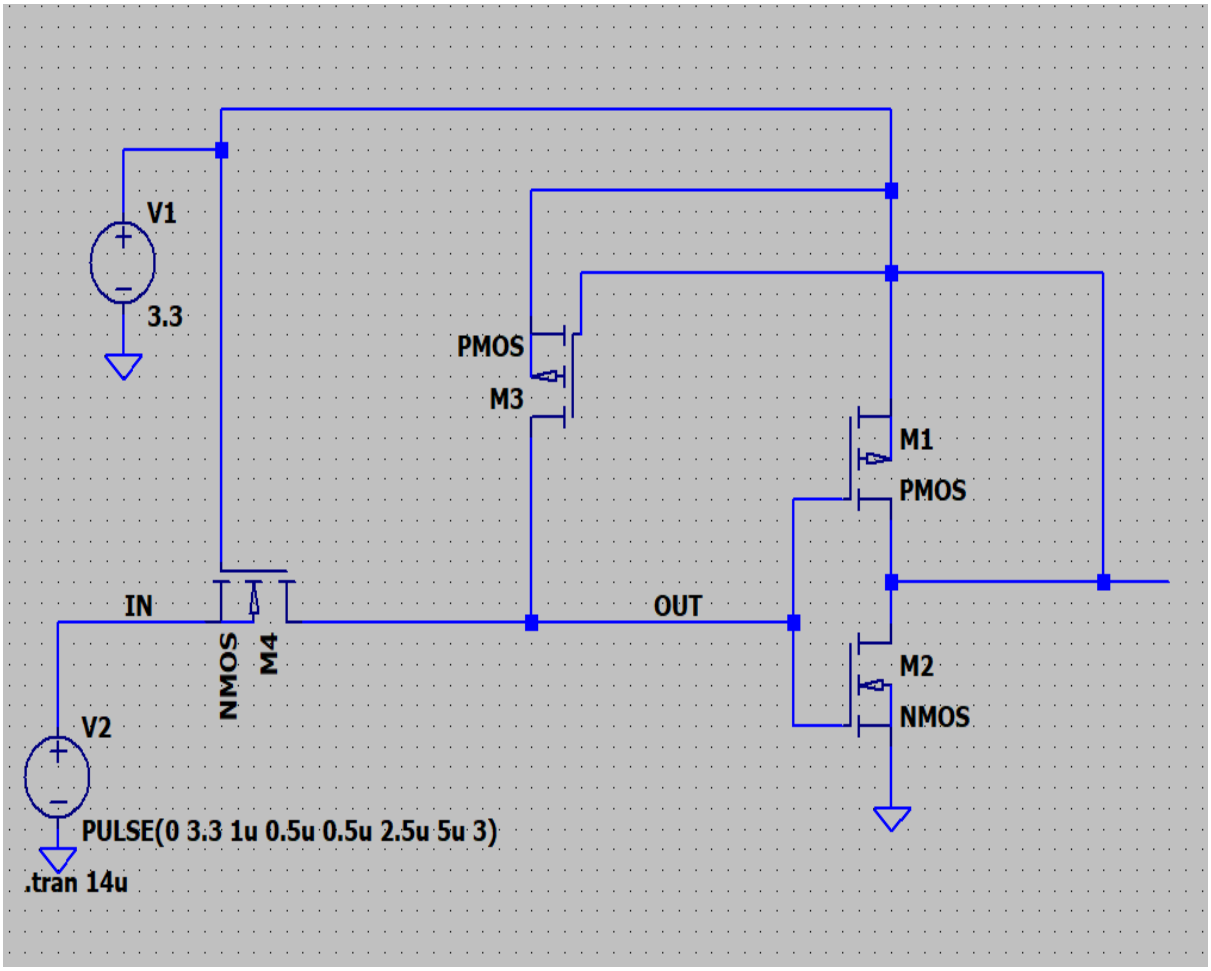

Figure 7: Circuit diagram of proposed technique

In the initial case, with the NMOS gate tied to V1 and source to 0V, the NMOS conduction requirement is Vgs ≥ Vtn. Since V1 = Vdd, then the gate-source voltage is Vdd - 0 = Vdd, which is greater than the threshold voltage, activating the NMOS transistor. The output of the NMOS is 0V, which is used as the inverter input. The inverter then generates a logic high (1) output, which is returned to the gate of the PMOS pass transistor, causing it to be switched off. Consequently, the output of the level restorer is 0V.

In the second case, with both the source and gate of the NMOS pass transistor attached to Vdd, the voltage between the source and gate of the NMOS transistor is Vdd - Vdd = 0V, which is subthreshold, shutting off the NMOS transistor. This results in the previously obtained voltage, |Vdd – Vtn|, at the inverter input. The CMOS inverter now produces an output of 0V, which is returned to the gate of the PMOS pass transistor. The feedback switches the PMOS transistor on so that it can pull the voltage up to Vdd. Because the voltage drop problem creates an output of |Vdd – Vtn|, the feedback-controlled PMOS pass transistor fills in this drop so that the full voltage level is returned.

IV. Simulation result

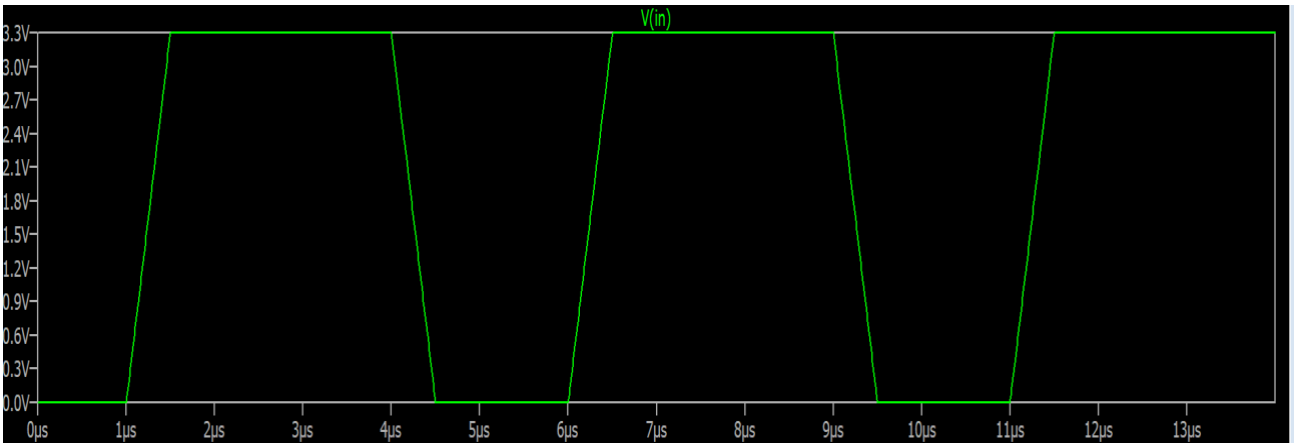

Figure 8: Input characteristics of proposed technique

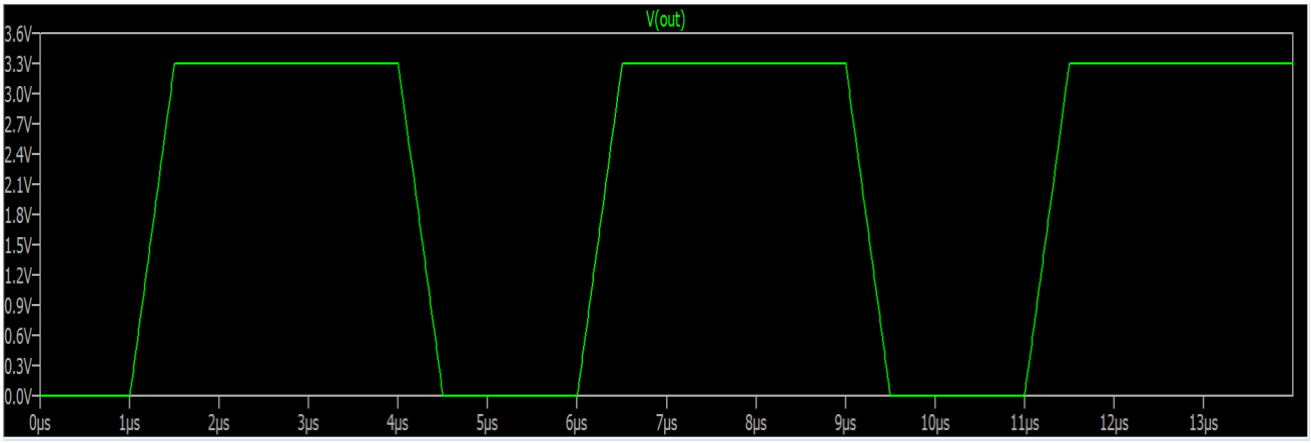

Figure 9: Output characteristics of proposed technique

IV. Comparative Analysis

Comparative analysis of conventional method and proposed technique is shown in table 10.

Parameters	Proposed Technique	Conventional Technique
Power dissipation	0.006 us	0.161 us
No. of transistors	4	1

Table 10: Comparative analysis between proposed and conventional technique

Comparative study of NMOS pass transistor and new technique through PMOS pass transistor has been performed here in terms of signal degradation. Propagation delay of new technique and conventional NMOS pass transistor has been compared and through the use of CMOS inverter circuit feedback with new technique has been enhanced by 96.2%. But due to the use of CMOS inverter circuit, circuit complexity has been regained. By using CMOS inverter circuit and PMOS pass transistor, transistor count has been boosted so area of new technique has been increased while applying new technique the level of output signal has been regained successfully

VI. Conclusion

The suggested method effectively overcomes the threshold voltage drop issue inherent in NMOS pass transistor-based circuits by combining a PMOS pass transistor with a CMOS inverter using feedback mechanism. By comprehensive comparative analysis, it has been seen that whereas NMOS pass transistors are plagued by signal degradation because of their inability to pass a strong logic high signal, the suggested method effectively restores the signal level, thus providing better performance and reliability. With an analysis of the propagation delay, it has been shown that the new method boosts the efficiency in signal transmission by 96.2%. The feedback presented by the CMOS inverter circuit to the PMOS pass transistor is pivotal in offsetting the voltage drop, thus strengthening the overall signal integrity. Increased circuit complexity and the number of transistors is the compromises that must be made for such an improvement in signal integrity, but at a cost of bigger area requirement. In spite of the compromises on circuit area and complexity, the technique presented in this paper presents a strong value in signal fidelity preservation and, therefore, provides a strong candidate for high signal fidelity applications. The combination of the CMOS inverter with the PMOS pass transistor bypasses the inefficiencies of the NMOS pass transistors very effectively, presenting a superior and more reliable method of restoring signals in digital circuits.

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